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This Week's Citation Classic

Dennard R H, Gaensslen F H, Yu H N, Rideout V L, Bassous E & LeBlanc A R.
Design of ion-implanted MOSFET's with very small physical dimensions.
IEEE J. Solid-State Circuits SC-9:256-68, 1974.
[IBM Thomas J. Watson Research Center, Yorktown Heights, NY]

Scaling relationships are presented which show how conventional MOSFET's can be reduced in size and which project the resultant performance in digital integrated circuits using small dimensions. Design principles, fabrication steps, and experimental results are given for 1 μm channel-length MOSFET's utilizing ion-implantation techniques. [The *SCI*® indicates that this paper has been cited over 145 times since 1974.]

R.H. Dennard
IBM
Thomas J. Watson Research Center
Yorktown Heights, NY 10598

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"In 1970, a small group at our laboratory, who had previously worked on field effect transistors (FET's), were organized into a new effort. We wanted to take advantage of potential advances in lithography techniques, particularly step-and-repeat optical projection or electron-beam pattern writing, which we felt could reduce typical dimensions used in integrated circuits from 5 μm to about 1 μm. D.L. Critchlow was the leader and principal architect of these ideas.

"One of the practical problems we had to face was how to design FET's with very small dimensions. We knew that FET's exhibited a precipitous (and undesired) drop in the gate voltage required to switch them when the source-drain spacing was reduced past a certain value, in those days about 4 μm. We understood this was related to the size of the depletion regions around the source and drain, which began to merge and interfered with the gate control. Considering how to reduce these depletion regions, and assessing the impact on other device properties, it soon became clear that there was a general way to design smaller devices which involved proportional scaling of a few key parameters. Reducing the applied voltage and increasing the silicon substrate doping concentration by a factor α causes the depletion regions to be reduced by that same factor. All the dimensions of the device can then be reduced by α, maintaining the same electric field patterns.

"It was a remarkably simple and concise concept, yet very powerful. It told us to expect a performance improvement of α times in our miniaturized circuits, and projected an α^2 reduction in power which allows the denser circuits to be properly cooled. We proceeded with further studies to confirm the theory by experiments and to understand the limits. This work was then presented at a major conference.[1]

"We continued to work in this field, building improved exploratory devices at 1 μm dimensions using ion implantation to control the doping levels in the critical region between source and drain. Then we published the paper which is often cited, including all the concepts of FET scaling which were first being introduced in a major journal.

"I believe that most of the citations to this paper refer to the portion involving scaling. Its acceptance is shown by the fact that small or miniaturized FET's are now universally called 'scaled' or 'scaled-down' devices. The paper in which this name first appeared is often cited in new papers to define the field of their work. Another reason for citing our paper is to show extensions, discuss limitations, or show alternate ways of designing devices and circuits. A later paper shows refinements we ourselves have made, along with measurements confirming the circuit performance levels.[2,3]

"On the whole, I am very pleased with the impact of this paper and believe that the frequency of citation is an indication of its merit. It was a factor in my being selected for the 1982 IEEE Cledo Brunetti Award. I would like to commend the other authors for their excellent contributions and cooperation."

1. **Dennard R H, Gaensslen F H, Kuhn L & Yu H N.** *Design of micron MOS switching devices.* Paper delivered at the IEEE International Electron Device Meeting, December 1972, Washington, DC.
2. **Dennard R H, Gaensslen F H, Walker E J & Cook P W.** 1 μm MOSFET VLSI technology: part II—device designs and characteristics for high-performance logic applications. *IEEE Trans. Electron Devices* ED-26:325-33, 1979.
3. ————————————————, 1 μm MOSFET VLSI technology: part II—device designs and characteristics for high-performance logic applications. *IEEE J. Solid-State Circuits* SC-14:247-55, 1979.

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